REMARKS

The Office Action objected to the drawings and rejected claims claims 1-9, 11, 14 and 19 under 35 U.S.C. 102(a) as anticipated by U.S. Patent No. 6,642,617 (Kawai) in view of *Active Substrates* by Steve Riches (Riches) and MCE Company Presentation (MCE). Claim 20 was rejected under 35 U.S.C. 102(a) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kawai. Claim 3 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE and Lin (U.S. Publication No. 6,806,578). Claim 10 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE, and *Electronic Packaging and Interconnection Handbook* by Charles A. Harper (Harper). Claims 12 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE, *Microchip Fabrication* by Peter Van Zant (van Zant). Claims 15 and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE, Pohjonen (U.S. Patent No. 6,462,950). Claim 17 was rejected under 35 U.S.C. 103 (a) as being unpatentable over Kawai in view of Riches, MCE, Pohjonen and Van Zant. Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE, Apel (U.S. Patent No. 6,727,761).

The Drawing Objection and Section 112 Rejections

The Drawings have been amended. Withdrawal of the objection and rejections is requested.

The Section 103 Rejection

In regards to claim 1, the Office Action asserts that Kawai discloses the following:

a) one or more active substrates (12a) comprising substantially transistors or diodes (10) formed thereon (For Example: See Figure 3 and Column 5 Lines 45 and 46);

b) one or more passive substrates (2a) comprising substantially inductors, capacitors or resistors (4) formed thereon (For Example: See Figure 3 and Column 4 Lines 17-20);

c) a plurality of bonding pads (15a and 5b) positioned on the active and passive substrates (For Example: See Figure 1);

d) bonding wires (6) connected to the bonding pads (For Example: See Figure 1).

The Office Action acknowledged that Kawai fails to disclose a plurality of active substrates, but asserts that:

However, Riches discloses a semiconductor device that has a plurality of active substrates (For Example: See Page 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include a plurality of active substrates as disclosed in Riches because it aids in providing a support for the interconnection of various components (For Example: See Page 1).

Additionally, since Kawai and Riches are both from the same field of endeavor, the purpose disclosed by Smiths would have been recognized in the pertinent art of Riches.

b) intra-substrate pads adapted to support wire-bonding within a substrate.

However, MCE discloses a semiconductor device that has intra-substrate pads adapted to support wire-bonding within a substrate (For Example: See Overview 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include intra-substrate pads adapted to support wire-bonding within a substrate as disclosed in MCE because it aids in providing interconnection to other components (For Example: See Overview 2).

Additionally, since Kawai and MCE are both from the same field of endeavor, the purpose disclosed by MCE would have been recognized in the pertinent art of Kawai.

Applicants respectfully traverse the rejection. Kawai relates to a semiconductor device with a SAW device chip provided on a passive element chip in which a passive element circuit including a transmission line is formed on a semi-insulating compound substrate having one surface set to have a ground potential electrode.

Here, neither Kawai, Riches, nor MCE shows as a plurality of bonding pads positioned on the active and passive substrates including intra-substrate pads adapted to support wire-bonding within a substrate. As shown in FIG. 1 of the instant application, each substrate 20, 30 and 40 may have **intra-substrate pads that allow wire-bonding to be done within a substrate**.

In contrast, MCE's Overview 2 shows that all wire-bondings are done between an active device (FPGA 2) and a silicon substrate serving as a base or pad to mount the active devices thereon. If the FPGA 2 corresponds to the substrate in accordance with the claim, then the MCE substrate 2 would not be a substrate in accordance with the claim, but would correspond to a pad such as the pad of claim 9. The MCE reference shows that the bonding wires are between the substrate and the base. However, MCE's Overview 2 does not show **intra-substrate pads that allow wire-bonding to be done within a substrate**. There are no intra-substrate pads on MCE's Overview – 2. MCE shows a single substrate mounted above a "motherboard" but does not show one or more active and passive substrates with **intra-substrate pads that allow wire-**

bonding to be done within a substrate Hence, neither Kawai, Riches nor MCE show the intra-substrate pads to support wirebonding within the substrate.

Moreover, the combination of Kawai, Riches, and MCE would result in an inoperable device. Riches and MCE disclose CMOS MCM substrates. One skilled in the art would not combine the CMOS substrates of Riches and MCE with the GaAs substrates of Kawai. The Kawai substrates need to be GaAs for both active and passive substrates for matching purposes such as impedance matching, among others. Moreover, the passive GaAs substrate provides precision passive circuitry that CMOS substrates cannot provide. Combining the Kawai passive and active GaAs substrate with Riches and MCE active CMOS substrates would be non-functional and the combination would not provide sufficient linearity to support a linear power amplifier. The CMOS substrate would not provide a low loss substrate. Further, the CMOS substrate would not be a semi-insulating substrate such as a GaAs substrate. The CMOS substrate would not provide the impedance matching that a GaAs substrate would provide. The combination of CMOS and GaAs circuits would not provide performance WiFi circuits such as power amplifiers. Hence, one skilled in the art would not combine Kawai with Riches or MCE.

Applicant notes that the present rejection does not establish *prima facie* obviousness under 35 U.S.C. § 103 and M.P.E.P. §§ 2142-2143. The Examiner bears the initial burden to establish and support *prima facie* obviousness. *In re Rinehart*, 189 U.S.P.Q. 143 (CCPA 1976). To establish *prima facie* obviousness, three basic criteria must be met. M.P.E.P. § 2142. First, the Examiner must show some suggestion or motivation, either in the Kawai reference or in the knowledge generally available to one of ordinary skill in the art, to modify the reference so as to produce the claimed invention. M.P.E.P. § 2143.01; *In re Fine*, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Secondly, the Examiner must establish that there is a reasonable expectation of success for the modification. M.P.E.P. § 2142. Thirdly, the Examiner must establish that the prior art references teach or suggest all the claim limitations. M.P.E.P. §2143.03; *In re Royka*, 180 U.S.P.Q. 580 (CCPA 1974). The teachings, suggestions, and reasonable expectations of success must be found in the prior art, rather than in Applicant's disclosure. *In re Vaeck*, 20 U.S.P.Q.2d 1438 (CAFC 1991). Applicant respectfully submits that a *prima facie* case of obviousness has not been met because the Examiner's rejection fails on at least two of the above requirements.

Under *Vaeck*, absent any evidence of a cited suggestion or reasonable motivation in the Norand reference, or knowledge of those skilled in the art, *prima facie* obviousness of the

independent claims (and those dependent therefrom) has not been established. As such, it is respectfully requested that the § 103(a) rejection of all claims be withdrawn and the claims be allowed.

Moreover, Kawai cannot render obvious any of the dependent claims that depend from allowable claim 1. The Office Action rejected claim 3 under 35 U.S.C. 103(a) as unpatentable over Kawai in view of Riches, MCE and Lin. Claim 10 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE and Harper. Claims 12 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE andvan Zant. Claims 15 and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE, and Pohjonen. Claim 17 was rejected under 35 U.S.C. 103 (a) as being unpatentable over Kawai in view of Riches, MCE, Pohjonen and Van Zant. Claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai in view of Riches, MCE and Apel.

First, as discussed above, the claims are allowable as none of the references show a device with a plurality of active substrates comprising substantially transistors or diodes formed thereon; one or more passive substrates comprising substantially inductors, capacitors or resistors formed thereon; a plurality of bonding pads positioned on the active and passive substrates including intra-substrate pads adapted to support wire-bonding within a substrate; and bonding wires connected to the bonding pads.

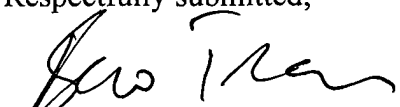
As Kawai fails to show a number of elements of the claims, withdrawal of the Section 103 rejection is requested.

CONCLUSION

Applicants submit that all claims are in condition for allowance.

If for any reason the Examiner believes that a telephone conference would in any way expedite prosecution of the subject application, the Examiner is invited to telephone the undersigned at (408) 528-7490.

Respectfully submitted,



Bao Tran
Reg. No. 37,955